



將 群 智 權 事 務 所

JIANQ CHYUN Intellectual Property Office

7F. -1, No. 100, Roosevelt Rd. Sec. 2, Taipei, Taiwan, R.O.C.

TEL: +886-2-2369 2800

E-mail: jianq@ms2.hinet.net website: www.JCIPGroup.com

FAX: +886-2-2369 7233/34

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March 28, 2003

CUSTOMER NO.: 31561

Attorney Docket No.: 7554-US-PA

Page(s): Cover +7

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FAX NO.: 002-1-703-872-9318

TO: UNITED STATES PATENT AND TRADEMARK OFFICE
Mrs. YOHA, CONNIE C.

MAR 28 2003

TECHNOLOGY CENTER 2800

MESSAGE: Enclosed please the Amendment in Response to the Office Action dated
January 30, 2003 for the Application No.: 10/064,266.

Note: The facsimile transmission is intended only for the use of the individual or entity to which it is addressed, and may contain information that is privileged, confidential and exempt from disclosure under applicable law. If the reader is not the intended recipient, or the employee or agent responsible for delivering the message to the intended recipient, you are hereby notified that any dissemination, distribution or copying of this communication is strictly prohibited. If you have received this transmission in error, please kindly notify us immediately, and return the original message to us at the above address. We greatly appreciate your cooperation.

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Customer No.: 31561
Application No.: 10/064,266

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

4/1/03

In re application of:

Application No.: 10/064,266

Filed: June 27, 2002

For: METHOD FOR FABRICATING FLASH
MEMORY) I hereby certify that this correspondence and all
) marked attachments are being deposited with the
) United States Postal Service as first class mail in
) an envelope addressed to: Assistant
Commissioner for Patents, Washington, D.C.
20231, on

Applicant: Chang et al.

Examiner: Chaudhari, Chandra P.

Art Unit 2813

No fee is believed to be due in connection with this amendment and response to Office Action.

AMENDMENT AND RESPONSE TO OFFICE ACTION

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Commissioner for Patents

Washington, DC 20231

MAR 28 2003

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Sir:

The Office Action mailed on January 30, 2003 (Paper No. 2) has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

REMARKS

1. (once amended) A method for fabricating a flash memory, comprising the steps of:
- forming a stacked gate structure and a source/drain on a substrate;
- forming an inter-layer dielectrics on the substrate; and